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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/789,190	HARGAN, EBRAHIM H.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-56 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14,17-19,24-35,37,38 and 40-56 is/are rejected.

7)☒ Claim(s) 15,16,20-23,36 and 39 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/29/2005.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-56 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 04/29/2005.

3. Information disclosed and list on PTO 1449 was considered.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-14,17-19,24-35,37-38,40-56 are rejected under 35 U.S.C. 102(e) as being anticipated by Royer (U.S. Patent No. 6,961,269).

Regarding claim 1, Royer discloses a device (Figure 1) comprising:

a plurality of data lines (Figure 7, 181);

a memory array for storing memory data (Figure 1, 102) ;

a conditioning data storage unit for storing conditioning data (Figure 7, 716, Column 9, lines 65-67, Column 10, lines 1-11) ;

a data selection circuit (Figure 1, 121) connected to the memory array (Figure 1, 102) and the conditioning data storage unit (Figure 1, 111, *Figure 7 shown conditioning data storage unit is a internal circuit of data path circuit coupled data selection circuit 121 by 165 and 167 as shown in Figures 1 and 7*) for selecting data between the memory data and the conditioning data;

a data transceiver circuit (Figure1, 127) connected to the data selection circuit for outputting to the data lines the data selected by the data selection circuit (Figure 1) ; and

a strobe transceiver circuit (Figure 1, 131) for providing timing information of the data outputted at the data lines (Figure 1, Figure 3, TIMING INFO, Column 5, lines 13-25).

Regarding claims 2-6, Royer discloses an output enable unit (figure e1, 118) having a driver enable circuit (Figure 2, WEN, REN, *these enable signals from 118 and coupled to 131 and 162, data and strobe transceiver circuits*) connected to the strobe and data transceiver circuits for simultaneously enabling the strobe and data transceiver circuits at a first time during a memory operation (Column 2, lines 34-44, and wherein the output enable unit further includes a data enable circuit (Figure 1, TM(0-n)) connected to the data selection circuit for enabling the data selection circuit to select the memory data at a second time during the memory access operation (Column 2, lines 49-56), and wherein the conditioning data storage unit includes multiple cells for storing multiple bits of data (Column 5, lines 12-25), and wherein the conditioning data storage unit includes only one cell for storing only one bit of data (Column 5, lines 12-25), and wherein the conditioning data storage unit is configured as a read-only storage unit (Figure 7, 716, Column 10, lines 1-11).

Regarding claims 7,14, Royer discloses a device (Figure 7) comprising:

a plurality of data lines (Figure 7, 181) ; a plurality of memory cells for storing memory data (Figure 1, 102) ; an output data path (Figure 7, 111) connected to the memory cells (Figure 1); a conditioning data storage unit (Figure 7, 716) for storing conditioning data; a plurality of multiplexers (Figure 7, 704,706, Column 9, lines 55-62), each of the multiplexers including a first input node connected to the output data path (Figure 7, *157 data path 111 coupled input mux 704*, Column 9, lines 55-62), a second input node connected to the conditioning data storage unit, and an multiplexing output node (Figure 7, 755A, coupled from 716 to mux 706, Column 9, lines 55-62); a plurality

of data transceivers (Figure 1, 162-0, 162-n) , each of the data transceivers connecting between the multiplexing output node and one of the data lines (Figures 1-2), and a plurality of strobe transceivers (Figure 2, 131-0, 141-M) for providing timing information of data outputted at the data lines (Figure 1, Figure 3, TIMING INFO, Column 5, lines 13-25).

Regarding claims 8-12, Royer discloses wherein the conditioning data storage unit includes a register connected to the second input node of the multiplexer (Figure 7, *conditioning data storage unit 716 coupled input node of mux 706*), and wherein the register includes a single register cell (Figure 7, Column 5, lines 13-25), and wherein the single register cell is configured to store a conditioning bit having a bit value of zero (Column 5, lines 16-19), and wherein the register includes multiple register cells (Figure 7, Column 5, lines 13-25), and wherein the conditioning data storage unit includes multiple register cells for storing multiple conditioning bits having multiple bit values (Column 5, lines 17-20), and wherein the conditioning data storage is configured such that the bit values of any two consecutive bits among the multiple conditioning bits are different from each other (Column 5, lines 16-25, logic one and zero).

Regarding claims 17-18, Royer discloses a driver enable circuit (Figure 1, 118) having an output node for providing a driver enable signal, wherein each of the data transceivers and each of the strobe transceivers connect to the same output node of the driver enable circuit (Figure 2, *data transceivers 162 and strobe transceivers 131-141 connected to the same enable signals WEN, REN*), and further includes a data enable circuit having an output node for providing the data enable signal, wherein each of the

multiplexers includes an enable node connected to the output node of the data enable circuit (Figure 7, multiplexers 704,706 *coupled enable signals Sin, and Sout*).

Regarding claims 19, 24-25, Royer discloses a system (Figure 8, 800) comprising:

a data bus (Figure 8, 810); a controller (Figure 8, 802) connected to the data bus; and a memory device (Figure 8, 804) connected to the controller via the data bus, the memory device including a plurality of data lines (Figure 7, 181) connected to the data bus; a memory array for storing memory data (Figure 1, 102) ; a conditioning data storage unit for storing conditioning data (Figure 7, 716, Column 9, lines 65-67, Column 10, lines 1-11); a data selection circuit (Figure 1, 121) connected to the memory array (Figure 1, 102) and the conditioning data storage unit (Figure 1, 111, *Figure 7 shown conditioning data storage unit is a internal circuit of data path circuit coupled data selection circuit 121 by 165 and 167 as shown in Figures 1 and 7*) for selecting data between the memory data and the conditioning data; a data transceiver circuit (Figure1, 127) connected to the data selection circuit for outputting to the data lines the data selected by the data selection circuit (Figure 1) ; and a strobe transceiver circuit (Figure 1, 131) for providing timing information of the data outputted at the data lines (Figure 1, Figure 3, TIMING INFO, Column 5, lines 13-25). More specifically, Royer discloses wherein the conditioning data storage unit is configured as a read-only storage unit (Figure 7, 716), and a number of register cells for storing multiple conditioning bits having multiple bit values (Column 5, lines 13-25), and wherein the conditioning data

storage unit is configured such that the bit values of any two consecutive bits among the multiple conditioning bits are different from each other (Column 5, lines 13-25).

Regarding claims 28-35, 37-38, 40, 41-50, 51-56 the apparatus discussed above would perform the method in claims 28-25, 37-38,40,41-50, 51-56.

Allowable Subject Matter

7. Claims 15-16, 20-23, 36, 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 15-16,20-23, 36, 39 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Royer (U.S. Patent No. 6,961,269), and others, does not teach the claimed invention having a storage node connects to ground or a voltage source as claims 15-16 disclosed, and the data transceiver circuit includes a plurality of multiplexers as claims 20-23 disclosed, and a method wherein outputting the memory data includes outputting the memory data at data line at data rate of at least one gigabits per second as claims 36 disclosed, and wherein before the conditioning bit is transferred, the data line has an initial signal level representing a bit value, and wherein the conditioning bit has a bit value unequal to the bit value of the data line as claim 39 disclosed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

3/09/2006